HDLGen-ChatGPT demos

- RISC-V components (some omitted) with series of HDLGen-ChatGPT project (.hdlgen files)
  - Project files

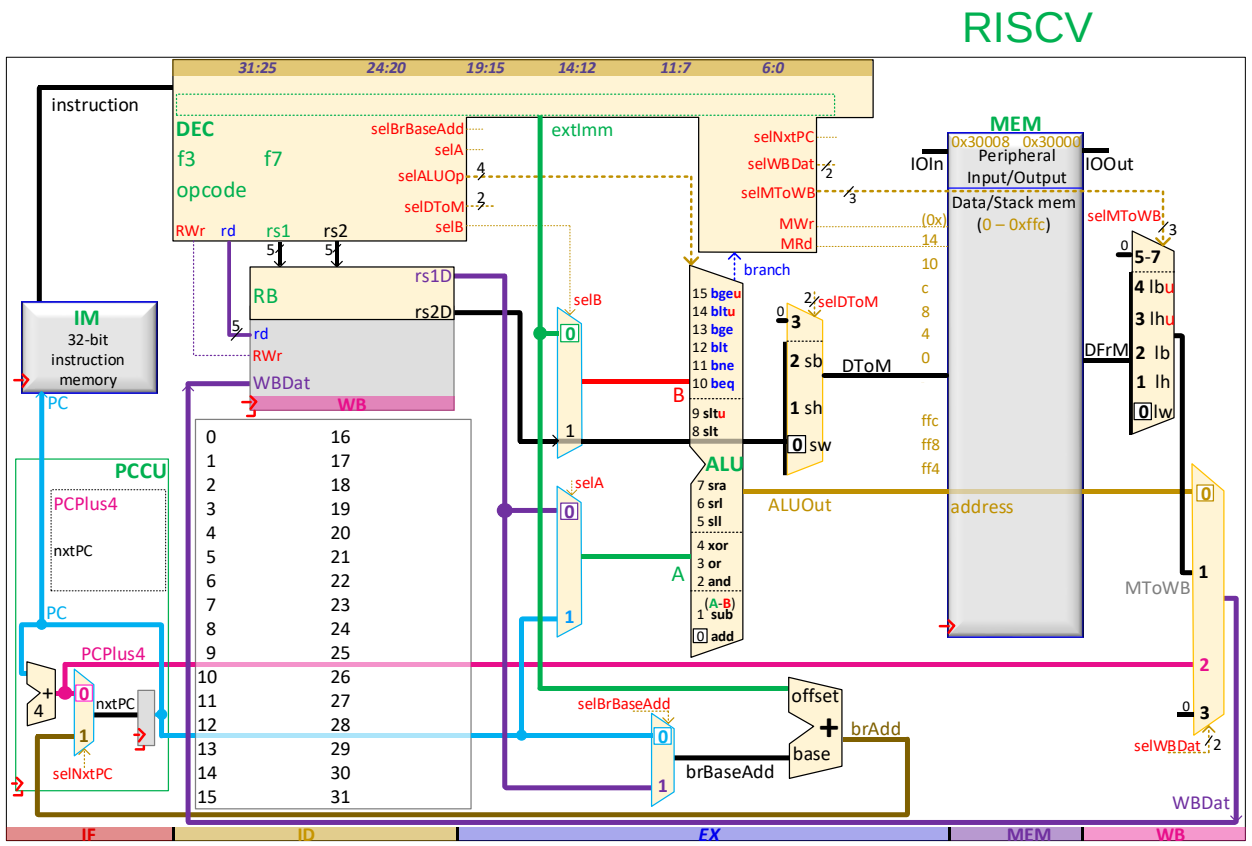
- 8-bit register, with high asserted chip enable (FD8CE)
  - Video demo
  - Presentation
  - Project files (HDLGen-ChatGPT project is FD8CE.hdlgen)

- Basic component AND21_1 Illustrating the HDLGen-ChatGPT functionality
  - Video demo
  - Presentation
  - Project files (HDLGen-ChatGPT project is AND21_1.hdlgen)

RV32I RISC-V Processor

- Video series to be uploaded soon

- RV32I RISC-V processor (**RISCV**)
  - Instruction Fetch (**IF**) stage
    - Instruction memory (**IM**)
    - Programme counter control unit (**PCCU**)
  - Instruction Decode stage (**ID**)
    - 32 x 32-bit register bank (RB)
    - Decoder (**DEC**)
  - Execution stage (**EX**)
    - **ALU** (initial demo focus)
    - **EX** mux and adder logic
  - Main memory (**MEM**)
  - Writeback stage (**WB**)



RV32I RISC-V architecture functional partition